Attorney Docket No.: YOR920040091US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re PATENT APPLICATION of:

Puneet Gupta et al.

Appln. No.:

Unknown

Art Unit:

Filed:

herewith

Examiner: Unknown

For:

INTEGRATED CIRCUIT LOGIC WITH

SELF COMPENSATING BLOCK

DELAYS

INFORMATION DISCLOSURE STATEMENT

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Sir,

Pursuant to the duty of disclosure under 37 C.F.R. §1.56, submitted herewith is an Information Disclosure Statement (IDS) including a Form PTO-1449 and a copy of one (1) non-patent publication. Pursuant to a Pre-OG Notice dated July 11, 2003 waiving requirement for copies of U.S. Patents and Published Applications, copies of Patents and Published Applications cited on the PTO-1449 are not included.

Since this IDS is being submitted with the application and prior to a first office action, no certification or fee is believed required, and the requirements of 37 C.F.R. §§1.97 and 1.98 are deemed to be fully met as to all documents submitted. Consideration of the submitted documents is respectfully requested.

Respectfully Submitted,

February 26, 2004

(Date)

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				First Named Inventor	Gupta et al.	
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U.S. PATENT DOCUMENTS							
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				First Named Inventor	Gupta et al.	
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		ORSHANSKY ET AL., A General Proabalistic Framework for Worst Case Timing Analysis, DAC 2002, 6/10/2002, Page(s) 556-61, Published in: New Orleans, LA			
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